

Branch Name:	Information and Communication Technology
Semester/Year:	Semester III / Second Year
Subject Title:	Digital Design
Subject Code:	1ET1070301
Pre-requisite:	Basic Electronics

Course Objectives:

- Apply the principles of Boolean algebra and k-map to manipulate and minimize logic expressions
- Apply two-level logic functions with AND, OR, NAND, NOR
- Design combinational circuits using decoders, ROM
- Design finite state machines using various types of flip-flops and combinational circuits
- Use the VHDL language for representation of digital signals

Teaching Scheme (Hours per week)				Evaluation Scheme (Marks)				
Lecture (L)	Tutorial (T)	Practical (P)	Credit	Theory (Marks)		Practical (Marks)		Total (Marks)
				University Assessment	Continuous Assessment	University Assessment	Continuous Assessment	
04	00	02	05	70	30	30	20	150

Subject Contents			
Sr. No	Topic	Total Hours	Weight (%)
1	Introduction to Number Systems and Boolean Algebra: Digital and Analog Basic Concepts, Some history of Digital Systems - Introduction to number systems , Binary numbers , Number Base Conversion - Complement Codes, Binary Arithmetic , Binary codes: BCD, Weighted codes -2421,8421,gray code - Binary Logic functions, Boolean Algebra, Theorems and Properties of Boolean Algebra	7	16%
2	Minimization techniques in digital Logic: Canonical forms, Generation of Switching Equations from Truth Table - K-map(Karnaugh map) 2 ,3,4 and 5 variables, K map with Don't care terms	6	15%
3	Design of Combinational Logic Circuits: Introduction to Combinational Circuits, Analysis and Design Procedure - Binary Adder, Subtractor, Carry Look Ahead Generator, Decimal Adder, Binary Multiplier - Decoder, Encoder, Priority Encoder, Digital Multiplexer, Magnitude Comparator	9	23%
4	Synchronous Sequential Circuits: Flip-flops- SR,D,JK,T - Analysis of Synchronous Sequential Circuit -	9	23%

	State Reduction and Assignment - Design of Synchronous Sequential Circuit: Sequence Detector for D,JK,T flip-flops - BCD Counter, Registers: Shift Registers, Analysis of Asynchronous Sequential Circuit: Transition Table, Flow Table		
5	Hardware Description Language: Introduction to HDL: Module Declaration, Gate delays, Boolean Expressions, User Defined Primitives - HDL models for Combinational Circuits: Gate Level Modeling, Data Flow , Behavioral Modeling - HDL flow Behavioural Sequential Circuits: HDL Models for Flip- Flops and Latches	9	23%

Course Outcome:

After learning the course the students should have knowledge about digital number systems and logic circuits. The student should be able to solve logic function minimization. The students should be able to understand and differentiate between combinational and sequential circuits such as decoders, encoders, multiplexers, de-multiplexers, flip-flops, counters, registers. They should be able to design using FSM. In the laboratory, they should be able to verify the functions of various digital integrated circuits. The students should be able to implement digital system in HDL programming.

Text Book:

1. John. M. Yarbrough, “Digital Logic: Applications and Design”, Cengage Learning, Reprint 2009.
2. Morris Mano, Michael D. Ciletti, “Digital Design with an Introduction to the verilog HDL”, Pearson Publications, Fifth edition 2014
3. Digital Logic and Computer Design By M Morris Mano, Fourth Edition, Prentice Hall Publication

List of Suggested Practical (including some of the practical based on HDL):

1. To study and verify performance of various Logic Gates.
2. To study and perform De-Morgan’s Theorem.
3. To perform NAND and NOR as Universal Gates.
4. Design and analyze Half Adder and Full Adder.
5. Design and analyze Half Subtractor and Full Subtractor.
6. Design and analyze Multiplexers.
7. Design and analyze Decoder and De-Multiplexer.
8. Design and analyze Encoder.
9. To study and perform 4 bit Magnitude Comparator.
10. To verify performance of RS and D Flip Flops.
11. To verify performance of JK and T Flip Flops.
12. To study and perform Decade Counter.
13. To study and perform Shift Register.
14. To study and verify performance of ROM design.