

Branch Name:	Information and Communication Technology
Semester/Year:	Semester VI / Third Year
Subject Title:	VLSI (Elective-I)
Subject Code:	1ET1070607
Pre-requisite:	Basic knowledge of basic and digital electronics

Course Objective:

- MOSFET: fundamentals, physics and fabrication
- VLSI Design Flow/methodologies, Design of digital designs using MOSFETs
- Exposure to Hardware Description Language during laboratory

Teaching Scheme (Hours per week)				Evaluation Scheme (Marks)				
Lecture (L)	Tutorial (T)	Practical (P)	Credit	Theory (Marks)		Practical (Marks)		Total (Marks)
				University Assessment	Continuous Assessment	University Assessment	Continuous Assessment	
03	00	02	04	70	30	30	20	150

Subject Contents				
Sr. No	Topic	Total Hours	Weightage (%)	
1	Introduction: Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, introduction to FPGA and CPLD, computer aided design technology.	4	8%	
2	Fabrication of MOSFET : Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design	4	8%	
3	MOS Transistor: Metal Oxide Semiconductor (MOS) structure, MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances	8	16%	
4	MOS Inverters: Static Characteristics: Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement and Depletion type MOSFET load), CMOS Inverter	7	13%	
5	MOS Inverters Switching characteristics and Interconnect Effects : Introduction, Delay-time definitions, Calculation of Delay times, Inverter design with delay constraints, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters	8	16%	

6	Combinational MOS Logic Circuits: Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs)	5	9%
7	Sequential MOS Logic Circuits : Introduction, Behavior of Bistable elements, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop	4	8%
8	Dynamic Logic Circuits : Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, High-performance Dynamic CMOS circuits	7	12%
9	Chip I/P and O/P Circuits : On chip Clock Generation and Distribution, Latch –Up and its Prevention	2	4%
10	Design for testability : Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques, built-in Self Test (BIST) techniques, current monitoring IDDQ test	3	6%
	Total	52	100%

Course Outcome:

After learning the course, the students will be able to understand the working MOSFET along with its fabrication. Based on inverter using MOSFET, students will learn about other digital logic design using MOSFET. Students will also learn some of the associated used in the area of VLSI.

List of Text Books:

1. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf Leblebici, Tata McGraw-Hill Publication

List of Reference Books:

1. Basic VLSI Design By Pucknell and Eshraghian, PHI, 3rd ed.
2. Introduction to VLSI Circuits & Systems – John P. Uyemura
3. Introduction to VLSI Systems by Mead C and Conway, Addison Wesley
4. Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic

List of Suggested titles of Experiments (If Any):

1. Introduction to programmable devices (FPGA, CPLD), Hardware Description Language (VHDL/verilog), and the use programming tool.
2. Implementation of basic logic gates and its testing.
3. Implementation of adder circuits and its testing.
4. Implementation 4 to 1 multiplexer and its testing.
5. Implementation of 3 to 8 decoder and its testing.
6. Implementation of 8 to 3 priority encoder and its testing.
7. Implementation of J-K and D Flip Flops and its testing
8. Implementation of sequential adder and its testing.
9. Implementation of BCD counter and its testing.
10. Implementation of two 8-bit multiplier circuit and its testing
11. Simulation of CMOS Inverter using SPICE for transfer characteristic.
12. Simulation and verification of two input CMOS NOR gate using SPICE.
13. To generate layout for CMOS Inverter circuit and simulate it for verification
14. To prepare layout for given logic function and verify it with simulations.

e-Resources (If any):

1. <http://nptel.ac.in/>