

Branch Name:	Signal Processing and Communication
Program Code:	ET214
Course Name:	VLSI Signal Processing
Course Code:	2ET2140105T
Pre-requisite Subject	Fundamentals of VLSI and Signal processing

Course Objective:

1. To study the design of folding and unfolding architectures, systolic architectures by students.
2. To study and understand the calculation of delay, global clock and latency for digital signal processing blocks of various architectures
3. To study the design of low power processing architectures using VLSI technology.
- 4.

Credit	Teaching Scheme Hours per week				Evaluation Scheme (Marks)								
					Theory (Marks)				Practical (Marks)				Total (Marks)
	L	T	P	Total	SEE		CCA		SEE		CCA		
					Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3	3	-	-	3	24	60	16	40		-	-	-	100

Subject Contents

Sr. No	Topic	Total Hours	Weight (%)
1	Iteration Bound: Introduction, Data-flow graph representations, Loop Bound and Iteration Bound, Algorithms for computing iteration Bound, Iteration Bound for multi-rate data flow graphs	6	20
2	Pipelining and Parallel Processing: Introduction, Pipelining for FIR digital filters, Parallel Processing, Pipelining and Parallel processing for low power	6	20
3	Retiming: Definitions and Properties, Solving Systems of inequalities, Retiming Techniques	4	10
4	Unfolding: Algorithm for unfolding, Properties of unfolding, Critical path, unfolding and retiming, Applications of unfolding,	7	15
5	Folding: Folding transformation, Register Minimizing Techniques, Registered minimizations in folded architectures, Folding of Multi-rate systems	7	15
6	Systolic Architecture Design: Systolic array design Methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-Matrix multiplication and 2D Systolic array design	5	10
7	Low Power Design: Theoretical background, Scaling versus Power Consumption, Power analysis, Power Reduction Techniques, Power Estimation approaches	4	10
Total		39	100

Review Presentation: The student is expected to spend minimum 2 hours per week (as mentioned in the time table) to refer at least two peer reviewed journal papers related to this domain/subject. The student is expected to identify issues/challenges and emerging trends in the domain/subject. Student is supposed to explore various video lectures (E.g. NPTEL) available in the domain/subject. Student is required to make a review-presentation on the work carried out for the same. Recommended sites for journal papers are (1) dl.acm.org (2) springer.com (3) sciencedirect.com

(4) [elsevier.com](#) (5) [ieeexplore.ieee.org](#) (6) [scholar.google.co.in](#) (7) [scopus.com](#) or others of same repute.

List of Text Books:

1. "VLSI Digital Signal Processing Systems", Keshab Parhi, Wiley India Edition

Reference Books:

1. "VLSI signal Processing" Keshab Parhi and Takao Nishitani
2. "Systolic signal processing systems" Eswartzlander CRC press
3. "Signal Processing Systems Design and Implementations", Elias S. Manolakos, IEEE, 1998
signal processing
4. "VLSI Physical Design Automation: Theory and Practice" by Sadiq M. Sait,
Habib Youssef, World Scientific Publishing.

Course Learning Outcomes (CLO): On completion of this course, the students will be able to:

CLO	Description	Bloom's Taxonomy Level
CLO1	Understand the concept and requirements of iteration bound	1 Remembering 2 Understanding
CLO2	Apply basics of pipelining and parallel processing and able design the system for high speed and low power requirements	2 Understanding 3 Applying
CLO3	Perform folding, unfolding and retiming operations on the given systems	2 Understanding 3 Applying
CLO4	Implement various algorithms based on systolic architectures.	3 Applying
CLO5	Implement various Systolic Architecture Design	3 Applying 4 Analyze
CLO6	Implement various Low Power Design	6 Create

Mapping of CLOs with POs & PSOs

Course Learning Outcomes	Program Outcomes (POs)												Program Specific Outcomes (PSOs)			
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	PSO 4
CLO1					L	M						H	H	M	L	
CLO2		H	M	M	L					L		H		M	L	
CLO3		M	H		L									H		L
CLO4		M	H		L			L					L		M	H
CLO5	H	M	H		L				L			H	L		M	H
CLO6	H	M	H		L							M	L		M	H

H: High, M: Medium, L: Low