

Branch Name:	Computer Engineering / Information Technology
Program Code:	ET103/ ET105
Course Title:	Computer Organization and Architecture
Course Code:	2ET1030403T
Pre-requisite Course:	Fundamentals of understanding basic concepts in mathematics, computer programming, and digital logic.

Course Objective:

1. To conceptualize the basics of organizational and architectural issues of a digital computer.
2. It begins with basic organization, design, and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations.
3. The core objective of this course is to have a thorough understanding of the basic structure and operation of a digital computer.
4. To analyze processor performance improvement using instruction level parallelism
5. This course aims to present various operation of the arithmetic unit, design Control Unit, different ways of communicating with I/O devices, memory system.

Teaching and Examination Scheme:

Credit	Teaching Scheme (Hours per week)				Evaluation Scheme (Marks)								
					Theory (Marks)				Practical (Marks)				Total (Marks)
	SEE		CCA		SEE		CCA						
	L	T	P	Total	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3	3	-		3	24	60	16	40	-	-	-	-	100

Course Contents:

Sr. No	Topic	Total Hours	Weight (%)
1	Basic structure of Computers: Block Diagram of General Purpose Computers and Fundamental Blocks of Computer, Computer types, Functional units, Basic operational concepts, VonNeumann Architecture, Timing and Control, Bus Structures, Instruction cycle, design of Accumulator Unit, Input-output and interrupt, Register Transfer language, Register Transfer, Bus and Memory Transfer, Multiprocessors and Multicomputer, Data representation, Fixed and Floating point, Error detection and correction codes. Arithmetic Micro-Operations, Logic Micro-Operations, Shift Micro-Operations, Arithmetic logical shift unit.	06	20
2	Programming The Basic Computer: Introduction, Machine Language, Assembly Language, assembler, Program loops Programming Arithmetic and logic operations, Subroutines	06	10
3	Input-Output Organization: Input-Output Interface Programmed I/O and Interrupt initiated I/O CPU-IOP communication Asynchronous Data Transfer, Modes Of Transfer, Priority Interrupt, DMA, Memory Memory Organization: Memory classifications, Memory Hierarchy , Various types of Main memories RAM ,ROM ,PROM ,EPROM ,EEPROM ,Associative Memory Various types of Auxiliary memories Magnetic tape Floppydisk HardDisks FlashMemory Cache Memory Virtual Memory	06	10
4	Fundamentals of Advanced Computer Architecture Parallel Architecture: Classification of Parallel Systems, Array Processors, Clusters, and NUMA Computers. Multiprocessor Systems: Structure & Interconnection Networks, Multi-Core Computers: Introduction, Organization and Performance. Pipeline And Vector Processing: Flynn's taxonomy, Flynn's Classification of Computers Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors.	05	15

5	Central Processing Unit Design: Introduction, Control Memory, design of control Unit, General Register Organization, Stack Organization, Instruction format, Addressing Modes, data transfer and manipulation, Reduced Instruction Set Computer (RISC), Complex Instruction Set Computer (CISC).	06	15
6	Arithmetic Processor Design: Introduction, Addition and subtraction, Multiplication Algorithms (Booth Multiplication Algorithm), Division Algorithms, Floating Point Arithmetic operations, Decimal Arithmetic Unit. Design Standards and Issues.	05	10
7	Advance topic in COA: Graphics Processing Unit (GPU), Introduction, GPU Memory Hierarchy, CUDA Programming Introduction, Code samples, Pentium 4 processor Organization and Architecture	03	20

Reference Books:

1. John P. Hayes, "Computer architecture and Organization", Tata McGraw-Hill, Third edition 1998.
2. V. Carl Hamacher, Zvonko G. Varanasic and Safat G. Zaky, "Computer Organization", Fifth edition, McGraw-Hill Inc, 1996.
3. Morris Mano, "Computer System Architecture", Prentice-Hall of India, 2000.
4. Behrooz Parhami, "Computer Architecture", Oxford Press.
5. William Stallings, "Computer Architecture and Organization Designing for Performance", Pearson Education.
6. David A. Patterson and John L. Hennessy, "Computer Organization and Design The Hardware/Software Interface" Morgan Kaufmann, 2013
7. Computer System Architecture: By M. Morris Mano.
8. Structured Computer Organization: By Tanenbaum.
9. Computer Organization: By Stallings.
10. Computer Architecture and Organization: By Hayes.
11. Microprocessor Architecture, Programming, and Applications with the 8085 - Ramesh S. Gaonkar Pub: Penram International.

E-Resources / Web Links

1. NPTEL Lecture Series
2. <http://www.intel.com/pressroom/kits/quickreffam.htm>
3. <http://williamstallings.com/COA6e.html>
4. <https://www.mbit.edu.in/wp-content/uploads/2020/05/computer-systems-Architecture.pdf>
5. https://ebooks.lpude.in/computer_application/bca/term_4/DCAP206_INTRODUCTION_TO_COMPUTER_ORGANIZATION_AND_ARCHITECTURE_DCAP502_COMPUTER_ORGANIZATION_AND_ARCHITECTURE.pdf

Course Learning Outcomes (CLO): On completion of this course, the students will be able to:

CLO	Description	Bloom's Taxonomy Level
CLO1	Basic structure of a digital computer	2 Understanding
CLO2	Understand the organization of the control unit and arithmetic and logical unit	1 Remembering
CLO3	Understanding summary of the Advanced Computer Architecture.	5, 3, 4 Evaluate, Applying, Analyze
CLO4	Write assembly language programs and identify the role and working of various functional	5, 3, 4 Evaluate, Applying, Analyze
CLO5	Recognize the importance of parallelism in computer architecture.	3 Applying, 2 Understanding
CLO6	To articulate design issues in the development of processors or other components that satisfy design requirements and objectives.	6 Creating
CLO7	Apply concepts and skills to solve problems using a low-level programming language	2, 3, 5 Understanding, Applying, Evaluate

Mapping of CLO with PO and PSO

Course Learning Outcomes	Program Outcomes (POs)												Program Specific Outcomes (PSOs)			
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CLO1		L	L				L					M	H	M	M	M
CLO2		M				L		M		H			H	M	M	M
CLO3					M			M					H	M	M	M
CLO4		M	M	M		M		M	M					M		M
CLO5				M	H	M	H	M	H						H	
CLO6										L		M		H		
CLO7	H	M	M	M			L						H	M	M	M

H: High, M: Medium, L: Low