

Branch Name:	Information and Communication Technology
Program Code:	ET107
Semester/Year:	Semester VI/ Third Year
Course Title:	VLSI (Professional Elective-III)
Course Code:	2ET1070604T
Pre-requisite:	Basic knowledge of basic and digital electronics

Course Objective:

1. To learn about MOSFET: fundamentals, fabrication.
2. Study the VLSI Design Flow/methodologies, Design of digital designs using MOSFETs.
3. To understand about Exposure to Hardware Description Language during laboratory.

Teaching and Examination Scheme:

Credit	Teaching Scheme Hours per week				Evaluation Scheme (Marks)								
					Theory (Marks)				Practical (Marks)				Total (Mark s)
	L	T	P	Total	SEE		CCA		SEE		CCA		
					Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
3	3	-	-	3	24	60	16	40	-	-	-	-	100

Subject Contents

Sr. No	Topic	Total Hours	Weightage (%)
1	Introduction: Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, introduction to FPGA and CPLD, computer aided design technology.	4	8
2	Fabrication of MOSFET: Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.	4	8
3	MOS Transistor: Metal Oxide Semiconductor (MOS) structure, MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances.	7	16
4	MOS Inverters: Static Characteristics: Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement and Depletion type MOSFET load), CMOS Inverter.	6	13

5	MOS Inverters Switching characteristics and Interconnect Effects: Introduction, Delay-time definitions, Calculation of Delay times, Inverter design with delay constraints, Estimation of Inter connect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters.	7	16
6	Combinational MOS Logic Circuits: Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs).	5	9
7	Sequential MOS Logic Circuits: Introduction, Behavior of Bistable elements, The SR latch circuit, 02Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop.	4	8
8	Dynamic Logic Circuits: Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, High-performance Dynamic CMOS circuits.	5	12
9	Chip I/P and O/P Circuits : On chip Clock Generation and Distribution, Latch-Up and its Prevention, Fin FET device.	2	4
10	Design for testability: Introduction, Fault types and models, Controllability and observability, AdHoc Testable design techniques, Scan –based techniques, built-in Self Test(BIST) techniques, current monitoring IDDQ test	2	6

List of Reference Books:

1. CMOS Digital Integrated circuits – Analysis and Design bySung – Mo Kang, Yusuf Leblebici, Tata McGraw-Hill Publication 4th edition 2019.
2. Basic VLSI Design By Pucknell and Eshraghian, PHI, 3rd edition 1995.
3. Introduction to VLSI Circuits & Systems–JohnP.Uyemura 2015.
4. Introduction to VLSI Systems by Mead Cand Conway, Addison Wesley 2003.
5. Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic 3rd edition 2017.

e-Resources (If any):

- 1.<http://nptel.ac.in/>

Course Learning Outcomes (CLO): On completion of this course, the students will be able to:

CLO	Description	Bloom's Taxonomy Level
CLO1	Overview of VLSI design methodology, Introduction, Fabrication Process flow	1 Remembering 2 Understanding
CLO2	Metal Oxide Semiconductor (MOS) structure, MOS Inverters: Static Characteristics	1 Remembering 2 Understanding
CLO3	MOS Inverters Switching characteristics and Interconnect Effects	2 Understanding
CLO4	Combinational MOS Logic Circuits, Sequential MOS Logic Circuits	2 Understanding 3 Applying
CLO5	Dynamic Logic Circuits, Chip I/P and O/P Circuits	2 Understanding 3 Applying
CLO6	Design for testability, Introduction, Fault types and models, Controllability and observability.	4 Analyze 5 Evaluate

Mapping of CLOs with POs & PSOs

Course Learning Outcomes	Program Outcomes (POs)												Program Specific Outcomes(PSOs)			
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3	PSO 4
CLO1	H		L					L			L		M		M	L
CLO2	M		M	H		L								L	L	
CLO3	M		M	H		L								L	M	M
CLO4					H	M		L		L		L		L		M
CLO5		M	H			L	L		M		L		M		H	H
CLO6		M	H			L			M				M		H	H

H: High, M: Medium, L: Low